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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,133	04/15/2004	Wagdi William Abadeer	BUR920030035US2	3132

24241 7590 11/03/2004

IBM MICROELECTRONICS
INTELLECTUAL PROPERTY LAW
1000 RIVER STREET
972 E
ESSEX JUNCTION, VT 05452

EXAMINER	
WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,133	ABADEER ET AL.	
	Examiner	Art Unit	
	Scott R. Wilson	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *1-8 and 20-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-13 and 16-18* is/are rejected.

7)☒ Claim(s) *14,15 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 9-19 in the response filed 23 September 2004 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 9 is rejected under 35 U.S.C. 102(b) as being anticipated by Nishimura et al.. Nishimura et al., Figures 5A – 5E, discloses a method of forming a semiconductor structure comprising the steps of providing a substrate comprising a plurality of levels (511), (512) formed thereupon, forming a metal-insulator-metal (MIM) capacitor (513), (514), (515) (col. 5, line 59) on an inter-level dielectric layer (512) in a first of the plurality of levels, and selectively forming an insulator layer (516) on said MIM capacitor, wherein portions, specifically, those below either of the interconnect layers (525), of the inter-level dielectric layer are insulator free.

As to claim 10, Nishimura et al., Figure 5A, discloses that the MIM capacitor comprises a bottom metal plate (513)(col. 5, line 55) adjacent the inter-level dielectric layer (512)(col. 5, line 53), a capacitor dielectric layer (514)(col. 5, line 56) on the bottom metal plate and a top plate (515)(col. 5, line 57) on the capacitor dielectric layer.

As to claim 11, Nishimura et al., Figures 5C and 5D, discloses that the step of selectively forming comprises forming said insulator layer (516) on said MIM capacitor and exposed portions of the inter-level dielectric layer, patterning a masking layer (520) on said insulator layer, and removing exposed portions,

(521) and the portion later to become interconnect layer (525), of said insulator layer to form said insulator-free portions.

As to claim 12, Nishimura et al. discloses (col. 5, lines 61-62) that the step of forming said insulator layer comprises chemical vapor deposition.

As to claim 13, Nishimura et al. discloses (col. 5, line 67) and (col. 6, line 7) that said removing step comprises reactive ion etching.

As to claim 16, Nishimura et al., Figure 5E, discloses that said insulator layer encapsulates the top metal plate (515) and the capacitor dielectric layer (514).

As to claim 17, Nishimura et al. discloses (col. 5, line 61) that said insulator layer (516) comprises silicon nitride.

As to claim 18, Nishimura et al. discloses (col. 5, line 53) that the inter-level dielectric layer (512) comprises silicon oxide.

Allowable Subject Matter

Claims 14 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed invention where portions of the bottom metal plate are removed in the removing step.

Claim 19 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed invention where said portions of the inter-level dielectric layer provide a path for diffusion of hydrogen and/or deuterium.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

srw
October 26, 2004

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800